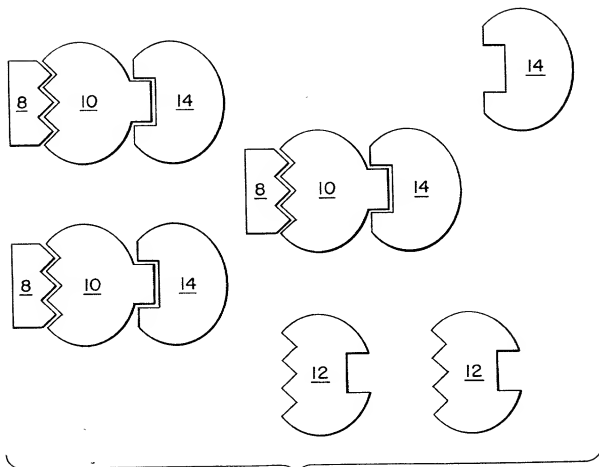
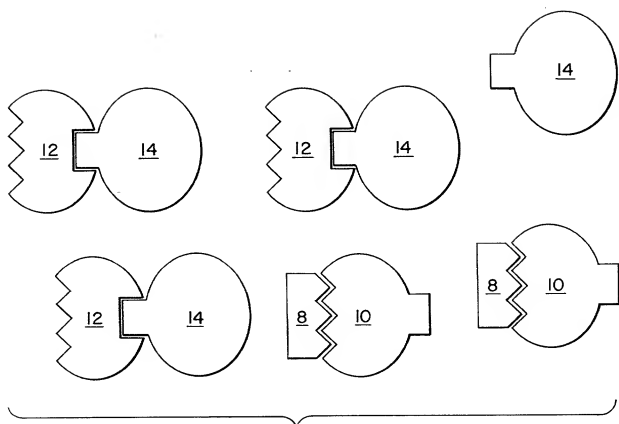


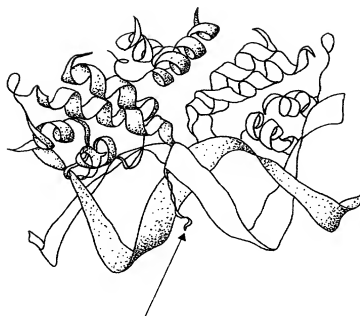
**FIG. 1A**



**FIG. 1B**

***FIG. 1C***

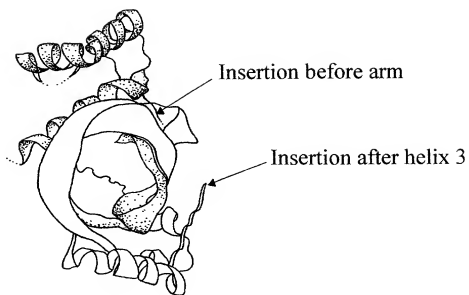
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Insertion before arm

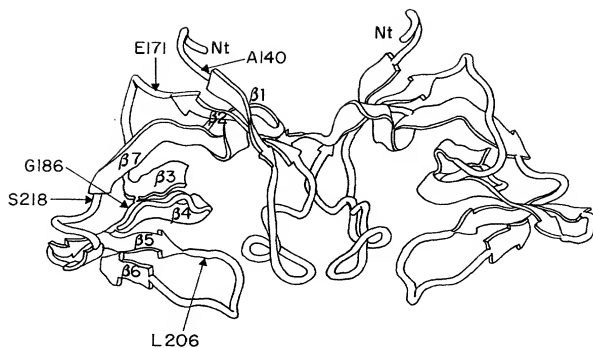
***FIG. 2***

10032827.041602



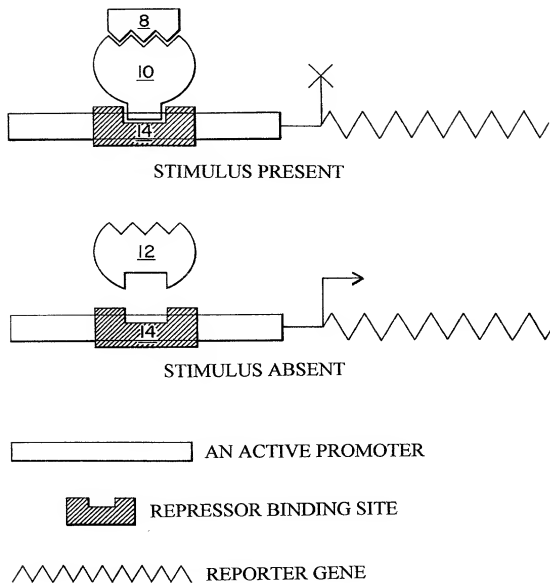
***FIG. 3***

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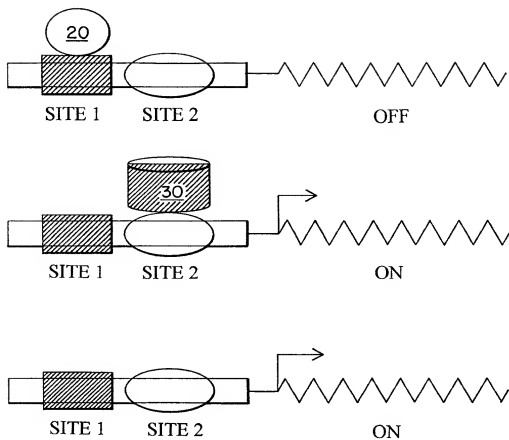


**FIG. 4**

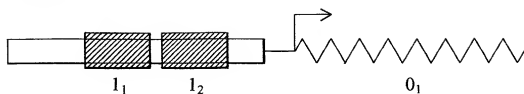
## SIMPLE BINARY SWITCH

*FIG. 5*

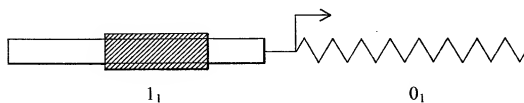
## FLIP-FLOP

**FIG. 6**

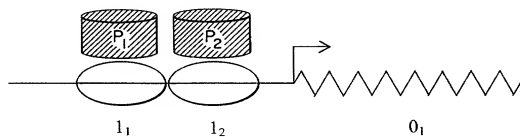
NOR GATE:

*FIG. 7A*

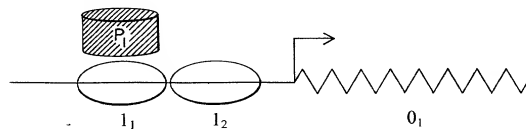
NOT GATE:

*FIG. 7B*

AND GATE:

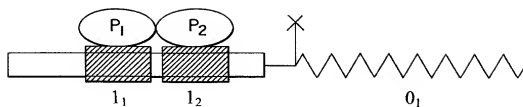
*FIG. 7C*

OR GATE:

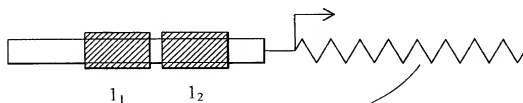
*FIG. 7D*



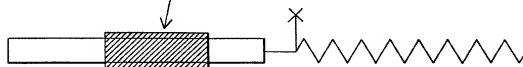
NAND GATE:

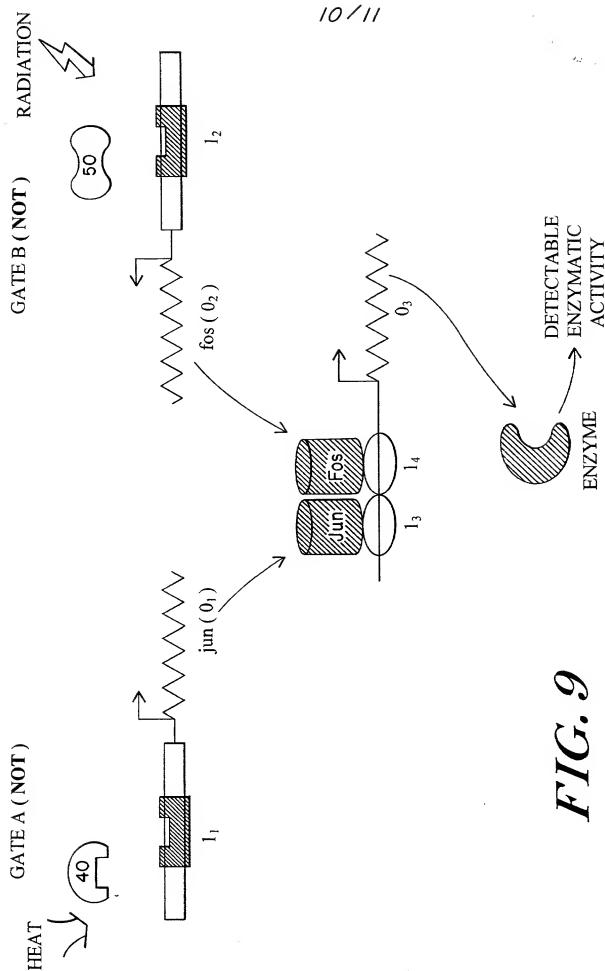
**FIG. 7E**

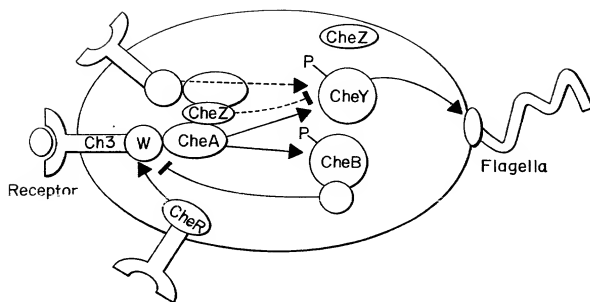
GATE A (NOR)



GATE B (NOT)

**FIG. 8**

**FIG. 9**

***FIG. 10***